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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **ITOH, Akio**

Group Art Unit: **2815**

Serial No.: **09/594,091**

Examiner: **Matthew Warren**

Filed: **June 15, 2000**

P.T.O. Confirmation No.: **8583**

For: **SEMICONDUCTOR MEMORY DEVICE HAVING PLANARIZED UPPER SURFACE  
AND A SION MOISTURE BARRIER (as amended)**

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**AMENDMENT UNDER 37 CFR §1.111**

Commissioner for Patents  
Washington, D.C. 20231

May 13, 2003

Sir:

In response to the Office Action dated **February 13, 2003**, please amend the above-identified application as follows:

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**IN THE CLAIMS:**

**Amend** claims 1, 5 and 12 as indicated below:

1. (Thrice Amended) A semiconductor device, comprising:
- a contact;
  - a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;
  - a first insulating film on top of the transistor;
  - a capacitor formed on the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower

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